**Lab 1: Logic Fundamentals**

Author: Seth Ricks

Date: 9/17/2025

Class: ECEN 340

**Purpose:**

1. To experience the construction of NAND and NOR gates at a transistor level.
2. To use signal generators and oscilloscopes to make timing measurements.

**Procedure:**

Part 1 – Use discrete NMOS and PMOS gates to build and test a NAND gate and a NOR gate.

Part 2 – Measure the output rise time, fall time, and propagation delay of a single 74HC04 inverter.

**Results/Report:**

Part 1:

In this part of the lab, we made a NAND and a NOR gate out of NMOS and PMOS transistors. First, we made the NAND gate, which is comprised of two PMOS in parallel (PUN) and two NMOS in series (PDN). This can be seen in the image below.

A close up of a device

AI-generated content may be incorrect.

Here is the resulting truth table from the NAND gate we created from the circuit:

NAND Truth Table Verification:

|  |  |  |  |
| --- | --- | --- | --- |
| x1 | x2 |  | f |
| 0 | 0 |  | 1 |
| 0 | 1 |  | 1 |
| 1 | 0 |  | 1 |
| 1 | 1 |  | 0 |

This is as expected, because the output is only true when one input is true, but not both.

Next, we created a NOR gate, which is the exact inverse of the NAND gate. It is made of two PMOS transistors in series (PUN), and two NMOS transistors in parallel (PDN).

A black electronic device with wires and wires

AI-generated content may be incorrect.

Here is the resulting truth table from the NAND gate we created:

NOR Truth Table Verification:

|  |  |  |  |
| --- | --- | --- | --- |
| x1 | x2 |  | F |
| 0 | 0 |  | 1 |
| 0 | 1 |  | 0 |
| 1 | 0 |  | 0 |
| 1 | 1 |  | 0 |

This is as expected, because the output is only true when neither input was true.

Part 2:

This part of the lab was focused on propagation delays. Using a 74LSO4 chips (the class ran out of 74HC04) we were able to measure the delay of a signal through 6 NOT gates. A picture of our circuit can be seen below:

A close-up of a circuit board

AI-generated content may be incorrect.

We achieved this by using a function generator and an oscilloscope. The function generator made two identical square waves. One was fed directly into the oscilloscope, and the other was fed through the inverter chip, and then into the oscilloscope. With the graph on the oscilloscope, we were able to see the propagation delay of the information. In other words, we saw how long it took for the signal to go through the chip. Because we used all the NOT gates in the chip, we had to divide the total delay by 6 to find the delay of a single gate. A table of our findings can be seen below.

\*NOTE: had 74LS04 instead of 74HC04

|  |  |
| --- | --- |
| 74LS04 Timing Measurements | |
| Rise time of any inverter output | 7.4 ns |
| Fall time of any inverter output | 3.75 ns |
| Prop Delay of all 6 inverters | 75ns |
| Prop Delay of single inverter (divided the above measurement by 6) | 12.5 ns |

The rising and falling results on the oscilloscope can be seen below. We used the notches on the scale to measure the propagation delays on both the rise and the fall times. I have also included the wide scale view of the signals, which you can notice are almost identical. It is not till you zoom in that you can see the small differences.

A white device with a screen and buttons

AI-generated content may be incorrect.A white electronic device with a blue screen

AI-generated content may be incorrect.

A white electronic device with a blue screen

AI-generated content may be incorrect.

**Conclusion:**

Our results of this lab were 99% in line with expected values. The only reason that we had data that was any different from expected was because we used the 74LS04 chip instead of 74HC04. This meant that our measured propagation delays were slightly different than expected.

The biggest difficulty that I had was understanding where to put the ground measurement out of the function generator and oscilloscope. I ended up putting them both together, and then to the ground of the inverter chip. This insured that there was a valid reference point for both the oscilloscope and the chip. This worked well and as intended.

Overall, I was able to have good hands-on experience with simple logic using transistors. This lab helped me understand better how logic gates worked, and how I might use them in the future.